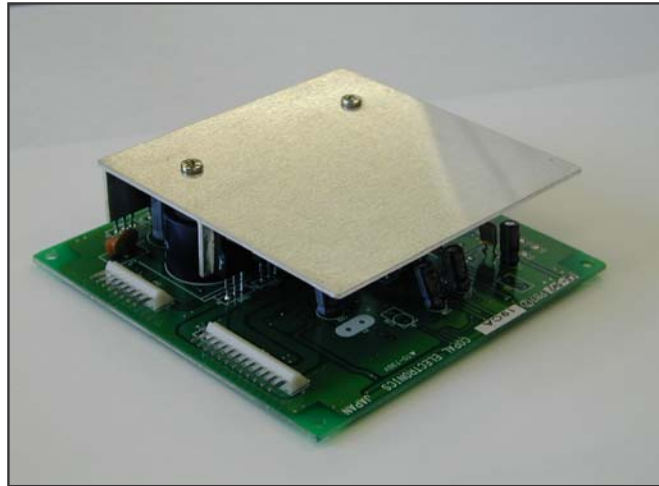


DRIVER PB (with power MOS FET)

■ For model PT60SRG ,PC60SRG



■ INTERFACE SPECIFICATION

(DRIVER FOR CN1 : BS7P-SHF-1AA,MADE BY J. S. T)

Pin No	MARK	FUNCTION	REMARKS
1	V	+24V	+24V DC
2	V	+24V	+24V DC
3	G	GND	GROUND
4	L	LOCKED	WHEN SYNCHRONIZED, IT GOES TO "L" OPEN COLLECTOR OUTPUT SYNCHRONIZED : LOW LEVEL LOW LEVEL : 0.8(V)MAX SINK CURRENT : 10(mA)MAX VOLTAGE APPLIED : 5.5(V)MAX
5	S	START/STOP	L:START H OR OPEN:STOP OPEN COLLECTOR INPUT START:LOW LEVEL LOW LEVEL:0.6(V)MAX.(V _{ce (sat)} =0.6V MAX) SOURCE CURRENT : 1.0(mA)MAX STOP : HIGH LEVEL OR OPEN HIGH LEVEL:4.0~5.3(V)
6	G	GND	GROUND
7	IX	INDEX	INDEX PULSE OUTPUT 74HC00 OUTPUT HIGH LEVEL OUTPUT VOLTAGE : 3.94V MIN LOW LEVEL OUTPUT VOLTAGE : 0.36V MAX
8	C	EXT.CLK	EXTERNAL CLOCK INPUT OPEN COLLECTOR INPUT LOW LEVEL:0.6(V)MAX.(V _{ce (sat)} =0.6V MAX) SOURCE CURRENT : 2.0(mA)MAX INPUT SIGNAL DUTY RAITO : 50%±10% THE FORMULA FOR EXTERNAL CLOCK FREQUENCY : f(Hz)=N(r/min)×3/60

DRIVER PB (with power MOS FET)

■ DIMENSIONS OF DRIVER PB

