

## DRIVER LK (with power IC)

■ For model PD60LA

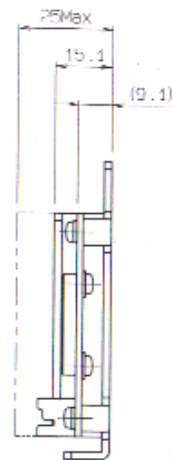
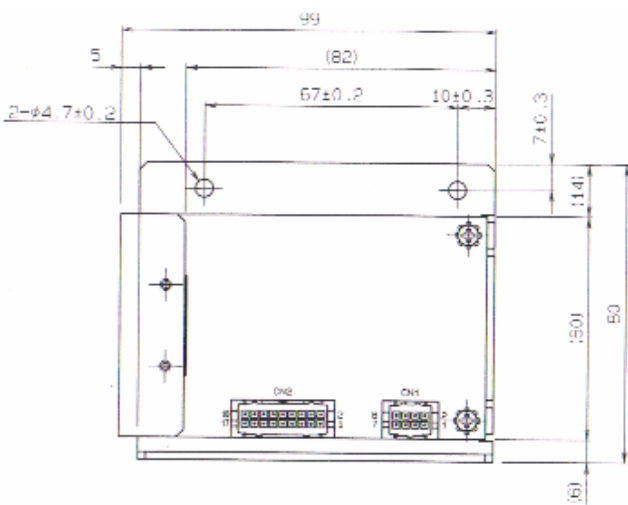


### ■ INTERFACE SPECIFICATION

(DRIVER FOR CN1 : BS7P-SHF-1AA,MADE BY J. S. T)

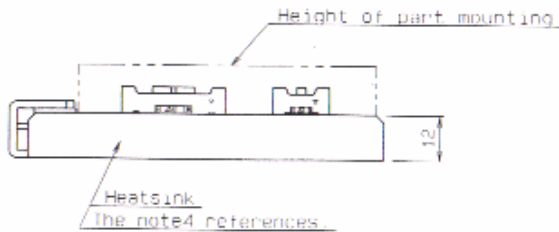
Pin No	MARK	FUNCTION	REMARKS
1	V	+24V	+24V DC ±10%
2	G	GND	GROUND
3	L	LOCKED	WHEN SYNCHRONIZED, IT GOES TO "L" OPEN COLLECTOR OUTPUT SYNCHRONIZED : LOW LEVEL LOW LEVEL : 0.8(V)MAX SINK CURRENT : 10(mA)MAX VOLTAGE APPLIED : 25(V)MAX
4	S	START/STOP	L:START H:STOP OPEN COLLECTOR INPUT) START:LOW LEVEL LOW LEVEL:0.8(V)MAX. (Vce (sat)=0.8V MAX) SOURCE CURRENT : 2.0(mA)MAX STOP : HIGH LEVEL OR OPEN HIGH LEVEL:ABOUT 3.25(V)
5	G	GND	GROUND
6	IX	INDEX	INDEX PULSE OUTPUT OPEN COLLECTOR OUTPUT VOLTAGE APPLIED : 9(V)MAX SINK CURRENT : 10(mA)MAX
7	F	N.C.	N.C.
8	C	EXT. CLK	EXTERNAL CLOCK INPUT OPEN COLLECTOR OUTPUT LOW LEVEL : 0.8(V)MAX. (Vce (sat)=0.8V MAX) SOURCE CURRENT : 5.0(mA)MAX HIGH LEVEL:ABOUT 4.7(V) INPUT SIGNAL DUTY RATIO : 50%±10% THE FORMULA FOR EXTERNAL CLOCK FREQUENCY $f(\text{Hz}) = N(\text{r}/\text{min}) \times 20/60$

### ■ DIMENSIONS OF DRIVER LK



**Notes**

1. CN1: Interface connector (JSI: B08B-XA05S-N-A)
2. CN2: Motor connector (JSI: B18B-XA05S-N-A)
3. Unless otherwise specified tolerances:  $\pm 0.5$
4. Isolation between heatsink and ground pattern.
5. Unit: in mm



CN1 (B08B-XA05S-N-A) interface		
Pin No.	Symbol	Signal
1	V	124V
2	G	GND
3	L	LOCKED
4	S	START/STOP
5	G	GND
6	IX	INDEX
7	C	EXT. CLK.
8	HL	N.C.