

Features

- Superior circuit protection
- Overcurrent & overvoltage protection
- Blocks surges up to rated limits
- High speed performance
- Small SMT package
- RoHS compliant*
- Agency recognition: ¶

Applications

- SLIC protection
- Cable & DSL
- MDU/MTU modems
- ONT
- Voice/DSL line cards

NIDEC COMPONENTS

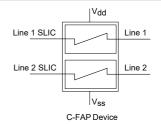
C-FAP-PL Series - C-FAP Fast Acting Protectors

General Information

The C-FAP-PL Series of NIDEC COMPONENTS C-FAP products are low capacitance dual bidirectional high speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.

In addition to overcurrent protection, an added feature is the voltage monitoring on the two lines. If the voltage on the line drops below V_{SS} then the voltage will trigger the device to switch to the blocking state

The C-FAP high speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during surge events. The C-FAP device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.



Agency Approval

Description UL File Number: E344793

* C-FAP-PL075 approval pending.

Industry Standards (in Conjunction with OVP Device)

Solutions available for GR-1089-CORE, ITU-T and a combination of both.

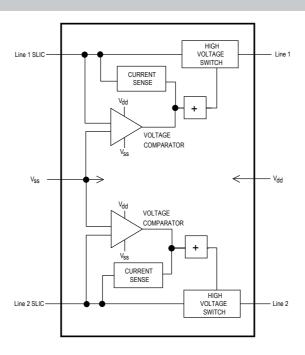
Absolute Maximum Ratings (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Number	Value	Unit
V _{imp}	Peak impulse voltage withstand with duration less than 10 ms	C-FAP-PL060-xxx-WH C-FAP-PL075-xxx-WH C-FAP-PL085-xxx-WH	600 750 850	V
V _{rms}	Continuous A.C. RMS voltage	C-FAP-PL060-xxx-WH C-FAP-PL075-xxx-WH C-FAP-PL085-xxx-WH	350 400 425	V
T _{op}	Operating temperature range	-55 to +125	°C	
T _{stq}	Storage temperature range	-65 to +150	°C	
T _{imax}	Maximum Junction Temperature	+125	°C	
ÉSD	HBM ESD Protection per IEC 61000-4-2 on line pads	±2	kV	

Electrical Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

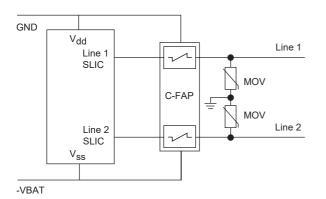
Symbol	Parameter	Part Number	Min.	Тур.	Max.	Unit
1.	Current required for the device to go from operating state to C-FAP-PLxxx-100-		100	150	200	mA
I _{trigger}	protected state	200	300	400	IIIA	
R _{C-FAP}	Series resistance of the C-FAP device		40	50	55	Ω
R _{match}	Package resistance matching of the C-FAP device #1 - C-FAF	device #2		±0.5	±1.0	Ω
t _{block}	Time taken for the device to go info current limiting				1	μs
IQ	Current through the triggered C-FAP device with 50 Vdc circuit	0.25	0.70	1.50	mA	
I _{ss}	Operating current with V _{ss} -50 V applied		100		μA	
V	Voltage below which the triggered C-FAP device will	C-FAP-PLxxx-100-WH	12	15	22	V
V _{reset}	transition to normal operating state	15	20	25	V	
V _{to}	Voltage threshold offset with 60 Hz applied voltage (V ss - Vline	_{SLIC}), with V _{ss} -50 V	-1.0		0.2	V
V_{ss}	Operating voltage range relative to V _{dd}	-180		-20	V	
R _{th(j-l)}	Junction to package pads - FR4 using minimum recommended		65		°C/W	
R _{th(i-l)}	Junction to package pads - FR4 using heat sink on board (6 cr		40		°C/W	

Functional Block Diagram



Reference Application

The C-FAP-PL Series are high-speed protectors used in voice/ VoIP SLIC applications. The maximum voltage rating of the C-FAP device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines NIDEC COMPONENTS C-FAP protection devices with a pair of Bourns® MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV.



Basic C-FAP Operation

The C-FAP device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The C-FAP device operates in approximately 1 µs - once line current exceeds the C-FAP device's trigger current I trigger. When operated, the C-FAP device restricts line current to less than 1 mA typically. When operated, the C-FAP device will block all voltages including the surge up to rated limits.

When the voltage on the SLIC output is driven below $(V_{bat} - V_{to})$ the C-FAP-PL series device switches to the blocking state, regardless of output current in the device.

After the surge, the C-FAP device resets when the voltage across the C-FAP device falls to the V_{reset} level. The C-FAP device will automatically reset on lines which have no DC bias or have DC bias below V_{reset} (such as unpowered signal lines).

If the line has a normal DC bias above V_{reset} , the voltage across the C-FAP device may not fall below V_{reset} after the surge. In such cases, special care needs to be taken to ensure that the C-FAP device will reset, with software monitoring as one method used to accomplish this. NIDEC COMPONENTS application engineers can provide further assistance.

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NIDEC COMPONENTS

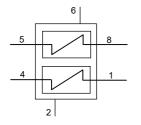
NIDEC COMPONENTS C-FAP Device Solution

Industry Standard	Surge & AC Tests	C-FAP Device P/N	Qty.	OVP Device P/N	Qty.
Telcordia GR-1089-CORE	5000 V, 500 A 2/10 μs 120V RMS, 25 A, 900 s	C-FAP-PL060-xxx-WH	1	MOV-10D201K	2
Enhanced Intra-building	1500 V, 100 A 2/10 μs 277V RMS, 25 A, 900 s	C-FAP-PL085-xxx-WH	1	MOV-10D431K	2
ITU-T	1500 V, 40 Ω 10/700 μ s 4000 V, 40 Ω 10/700 μ s 230 V rms 10 Ω -1000 Ω , 900 s 600 V rms 600 Ω , 1 s	C-FAP-PL060-xxx-WH	1	TISP4400M3BJ	2
K.20, K.21, K.45 Basic	1500 V, 40 Ω 10/700 μs 4000 V, 40 Ω 10/700 μs 230 V rms 10 Ω -1000 Ω , 900 s 600 V rms 600 Ω , 0.2 s	C-FAP-PL075-xxx-WH	1	MOV-10D361K	2
ITU-T	1500 V, 40 Ω 10/700 μs 6000 V, 40 Ω 10/700 μs 230 V rms 10 Ω -1000 Ω , 900 s 600 V rms 600 Ω , 0.2 s 600 V rms 600 Ω , 1 s 1500 V rms, 200 Ω 2s	C-FAP-PL060-xxx-WH	1	TISP4500H3BJ	2
K.20, K.21, K.45 Enhanced	1500 V, 40 Ω 10/700 μs 6000 V, 40 Ω 10/700 μs* 230 V rms 10 Ω -1000 Ω , 900 s 600 V rms 600 Ω , 0.2 s 600 V rms 600 Ω , 1 s* 1500 V rms, 200 Ω 2s*	C-FAP-PL085-xxx-WH	1	MOV-10D391K	2
Telcordia GR-1089-CORE Intra-building and ITU-T K.20, K.21, K.45 Enhanced	5000 V, 500 A $2/10$ μs 120 V RMS, 25 A, 900 s 1500 V, 40 Ω $10/700$ μs 6000 V, 40 Ω $10/700$ μs 230 V rms 10 Ω -1000 Ω , 900 s 600 V rms 600 Ω , 0.2 s 600 V rms 600 Ω , 1 s* 1500 V rms, 200 Ω $2s$ *	TBU-PL085-xxx-WH	1	MOV-10D391K	2

 $^{^{\}star}$ GDT Special Test Protector with DC breakdown (DCBD) of less than 330 V .

Note: The Le9500, Le9520 and Le9530 (VE950 series) require a 200 mA I $_{trigger}\,$ C-FAP device for normal operation.

Device Pin Out



Pad Designation

Pad #	Pin Out
1	Line 1
2	$V_{ m dd}$
3	Not Used
4	Line 1 SLIC

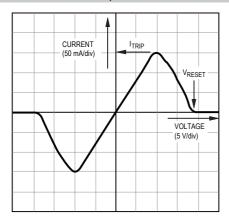
Pad #	Pin Out
5	Line 2 SLIC
6	V_{SS}
7	Not Used
8	Line 2

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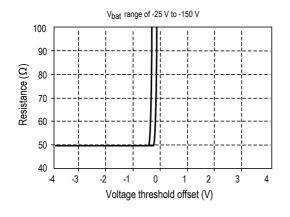
NIDEC COMPONENTS

Performance Graphs

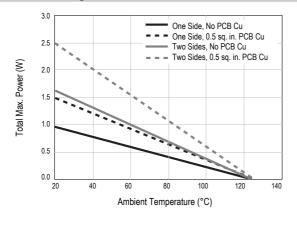
Typical V-I Characteristics (C-FAP-PL085-200-WH)



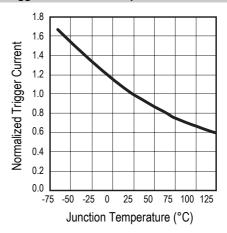
Tracking Voltage Characteristics



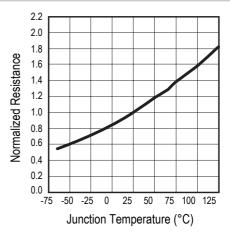
Power Derating Curve



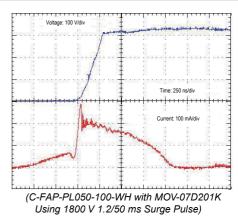
Typical Trigger Current vs. Temperature



Typical Resistance vs. Temperature

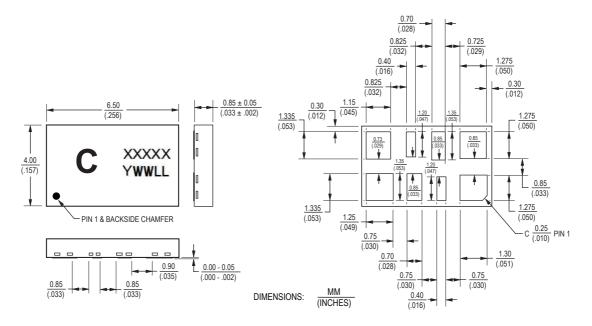


Typical Surge Response



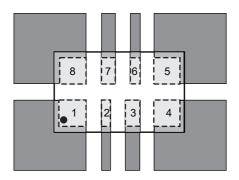
Specifications are subject to change without notice. Customers should verify actual device performance in their specific applications.

Product Dimensions



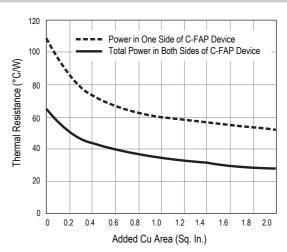
Recommended Pad Layout

C-FAP protectors have matte-tin termination finish. The suggested layout should use Non-Solder Mask Define (NSMD). The recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with a stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.



Dark grey areas show added PCB copper area for better thermal resistance.

Thermal Resistance vs Additional PCB Cu Area

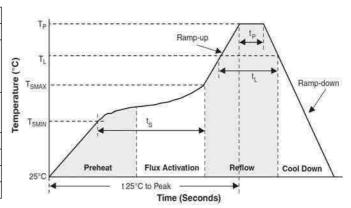


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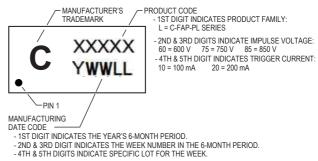
Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.

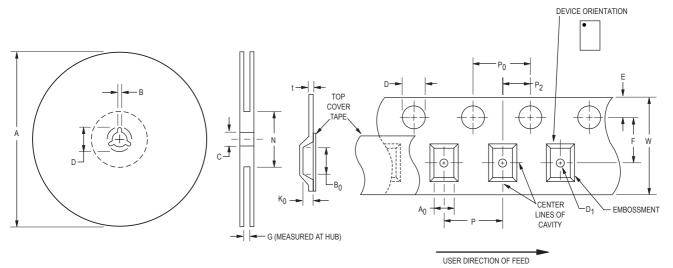


How to Order C-FAP - PL 085 - 100 - WH C-FAP Product Series PL = Dual Bidirectional Series Impulse Voltage Rating 060 = 600 V 075 = 750 V 085 = 850 V Trigger Current 100 = 100 mA 200 = 200 mA Hold to Trip Ratio Suffix W = Hold to Trip Ratio

Typical Part Marking



Packaging Specifications



QUANTITY: 3000 PIECES PER REEL

	4	В		С		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
326	330	1.5	2.5	12.8	13.5	20.2		16.5	102
$\overline{(12.835)}$	(13.002)	(.059)	$\frac{2.5}{(.098)}$	(.504)	(.531)	(.795)	-	(.650)	(4.016)

	Α	.0	В	80))1		=		=
ı	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
	4.30 (.169)	4.50 (.177)	6.70 (.264)	6.90 (.272)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)
	K	0	1)	P ₀ P ₂		t		V	V		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
	1.0	1.2	7.9	8.1	3.9	4.1	1.9	2.1	0.25	0.35	15.7	16.3
	(.039)	(.047)	(.311)	(.319)	(.159)	(.161)	(.075)	(.083)	(.010)	(.014)	(.618)	(.642)

DIMENSIONS: $\frac{MM}{(INCHES)}$

Revision History

Date	Rev.	Reason
10/12/2010	Α	Initial issue
05/15/2012	A1	Updated Performance Graphs and Packaging Specifications
02/13/2017	В	Change marking.
04/03/2023	С	Change our company name.

Revision : C Issue date : 04/03/2023